Wideband CDMA Smart Antenna Measurement System

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Abstract

Computer simulations of mobile communication systems often use ideal or simple channel propagation models. This assumption is sufficient for relative comparison of algorithms or for testing overall functionality, but insufficient when the actual performance in a physical environment is required. In order to perform physical experiments, a low-cost modular transmitter and receiver link for the uplink of a wideband CDMA system is presented. The transmitter is programmable, allowing varying PN chip-rates and PN code sequences, and the receiver can simultaneously acquire 16000 samples per antenna element at 5 samples per PN chip. The complete system can operate within the frequency range of 1-2 GHz, with multiple mobile transmitters and a multiple element antenna array basestation. Preliminary result includes one successful link tested at the 1.9 GHz frequency band, plus several further field experiments are proposed.

1 Introduction

A wideband CDMA (WCDMA) measurement system operating in the 1.9 GHz band using a smart antenna system is being designed and constructed. In this paper, we first discuss the low-cost modular approach employed in our system design, and then describe measurements obtained verifying the system design. The system offers high chip-rate and data storage for offline signal processing applicable to the uplink of a cellular communication system. It consists of a basestation antenna array and multiple mobile transmitters. Several previous approaches are discussed in the next section, followed by our system description in the third section. Physical experiments which will be performed on our testbed are proposed in the last section.

2 Previous Work

Several research groups have designed and conducted field testing in the 1.8 - 2.0 GHz frequency band [2] [7] [8] [11]. As each group's hardware, setup and objectives differ, their systems' capabilities and limitations also vary; in particular, none has employed WCDMA with multiple transmitters. In order to identify the novel aspects of our system, it is important to review previous work in the open literature relevant to our objectives.

Muhamed and Rappaport used a 6-element array for DOA (direction-of-arrival) estimation. The transmitted signals were CW tones and sampled at the receiver with 6 kHz analog-to-digital converter (ADC) [7]. Okamoto and Xu tested spatial signature variation, angle spread, beamforming by sending coded voice data over an RF channel at 1.8 GHz. Their system has 4 or 8 antenna elements and a sampling rate of 3.072 MHz [8]. The Communications Research Laboratory (CRL) of McMaster university built a smart antenna system equipped with one mobile transmitter and an 8-element circular array.

On a larger scale, Savahashi and Adachi of NTT Mobile Communications network INC. in Japan, and Wilson et al. of Institute for Telecommunication Sciences (ITS) in Colorado, performed experiments on WCDMA systems. Savahashi and Adachi's testbed includes a 2-element antenna, 4-finger Rake combining, fixed PN chip rate (15 MHz) and spreading code (256-chip orthogonal Gold sequence), and a sampling rate of 60 MHz using an 8-bit ADC [11]. While they studied BER performance and power delay profile in Rayleigh fading, ITS evaluated received signal strength and diversity combining algorithms, e.g. Selection, MRC (maximum ratio combining) and ORC (optimum ratio combining). A maximal length code sequence at 10 Mcps over PCS band was transmitted, and received signal was digitized at an IF frequency with a sampling rate of 40 Msps [2].

3 System Description

3.1 Introduction

Our existing system is a prototype WCDMA mobile system consisting of two programmable mobile transmitters (TX), and one 2-element antenna array basestation (BS) capable of data collection. We employ a low-cost modular approach in hardware system design; off-the-shelf components are chosen whenever applicable and possible to reduce cost as well as development time.

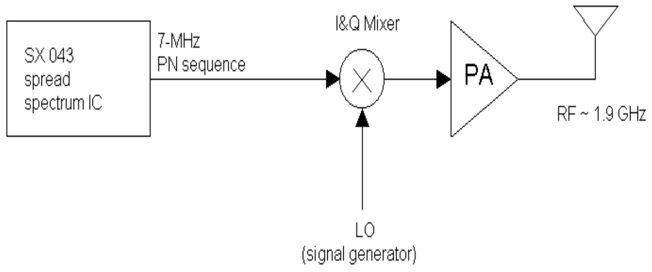

Figure 1: Direct RF transmitter link design

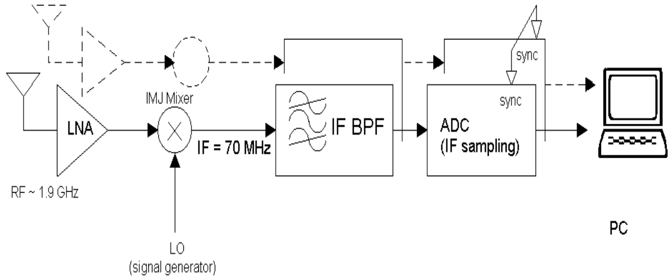

Figure 2: Digital Receiver link design

The transmitter is composed of a SX043 spread spectrum ASIC, a direct RF modulator, a power amplifier and an antenna. The spread spectrum IC has a programmable chip rate up to 64 Mcps, and three types of PN sequences to choose from; namely Gold, maximal length, and Barker codes. Square pulses are used to maintain our low cost objective since pulse shaping operations at high chip-rates require intensive DSP processing power. First, we program the SX043 to generate a 7-MHz PN sequence, which is then upconverted directly to RF centered at 1.9 GHz, and transmitted after power amplification (see Figure 1).

The basestation consists of a RF LNA, a mixer, an IF bandpass filter, and a digital receiver with a fast ADC. The incoming RF signal passes through a one-stage downconversion from RF to IF handled by the image-rejection mixer, then bandpass filtered before analog-to-digital conversion. The ADC is capable of IF wideband digitization at a speed up to 64M samples per second (sps). Currently we have chosen 35 Msps resulting in 5 samples per chip. The raw data are stored on hard-disk through a parallel port on a PC (see Figure 2).

Utilizing this receiver setup, we can obtain synchronized snapshots of transmitted signals. Synchronous sampling is achieved by external clocking of the ADC as shown by the "sync" line in Figure 2. Other system synchronization issues are discussed in Section 3.4.

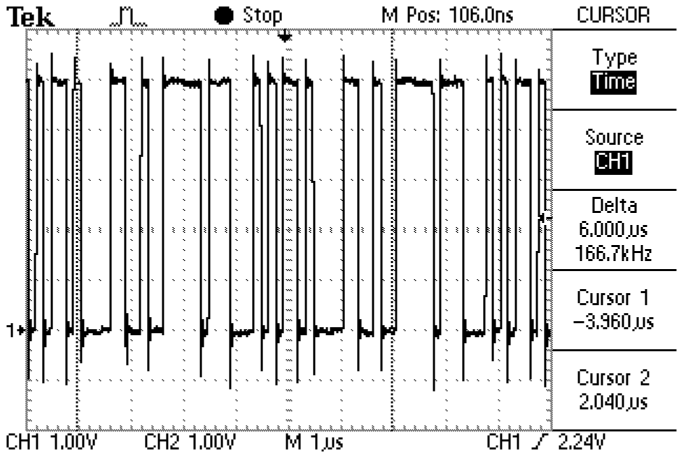

Figure 3: Baseband PN chip waveforms

3.2 Sampling and Data Collection

Oversampling provides several benefits in system design. It minimizes the requirements of the anti-aliasing filter by shifting the copies of spectrum of the sampled signal further apart. In addition, oversampling leads to an additional SNR gain because the distribution of noise is spread wider in bandwidth as the sampling rate increases[3][13].

The IF frequency is 70 MHz and by sampling at 35Msps, the 7 MHz bandpass signal is directly downconverted from IF to baseband. This process is usually called direct bandpass sampling[13]. By avoiding analog and digital demodulation, direct bandpass sampling reduces the complexity of the receiver and offline data processing. Direct bandpass sampling can be successfully employed since the IF carrier is only one order of magnitude larger than the signal bandwidth.

For data collection, the ADC's evaluation board has a 16K FIFO buffer which limits the maximum number samples to 16K per snapshot of incoming signal. The ADC control software has the option to save data in batches of 1K, 2K, 4K, 8K or 16K in ASCII format. All the received data stored on PC can be analyzed in matlab for post processing.

3.3 System Link Analysis and Testing

Referring to the transmitter link in Figure 1, the SX043 IC produces 7MHz rectangular chip waveforms as shown in Figure 3. The chip waveforms are then modulated to the RF frequency at 1.9 GHz. At the output of the modulator the peak signal power is roughly -10 dBm (see Figure 4). And at the antenna, after a power amplification gain of 26dB, the peak signal power increases to +16 dBm.

The link analysis for the receiver includes receiver noise

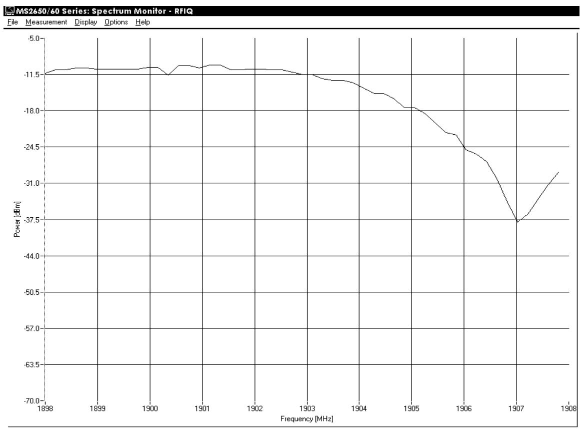

Figure 4: RF spectrum at modulator output

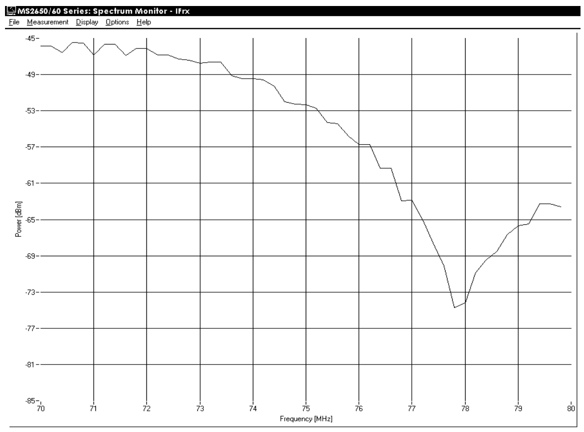

Figure 5: Received signal spectrum at IF

floor, sensitivity and dynamic range. The receiver noise floor is calculated as follows [5]:

$$
\begin{aligned}
P_{rn} &= kT + 10\log(B) + NF_{dB} \qquad (1)\\
&= -174dBm + 71.76dB + 1.75dB\\
&= -100.49dBm
\end{aligned}
$$

where $kT = -174dBm$ at room temperature, $B = 15MHz$ (bandwidth), and NF = receiver noise figure = $1.75dB$. And the receiver sensitivity S_r is:

$$
\begin{aligned}
S_r &= P_{rn} + \frac{E_b}{N_o} + \text{implementation loss} \qquad (2)\\
&= -100.49dBm + 6.8dB + 1.0dB\\
&= -92.69dBm
\end{aligned}
$$

where E_b/N_o is the SNR required for demodulation which we have chosen to correspond to a BER of 10^{-3} for BPSK demodulation.

Another important specification in digital receiver design is the SFDR (suprious free dynamic range) of the A/D converter. Non-linearities in the ADC cause spurious responses in the ADC's output spectrum. SFDR indicates the ability of an ADC to simultaneously detect a small signal with the presence of a large interference signal[13]. The SFDR specifications of the ADC is -111dBm with dither[3]. If the tolerable C/I ratio is 18 dB, then the minimum signal level is -93 dBm at the A/D converter or -103.5 dBm (system gain is 10.5 dB) at the antenna. The minimum signal level is constrained by the receiver sensitivity at about -92 dBm. With maximum input to the ADC converter at 0 dBm, the dynamic range of the receiver chain is about 92 dB.

A simple test of the functionality of the system was performed by placing the receiver at a close distance of roughly 1 metre from the transmitter. The peak signal power measured at IF, referred to the receiver antenna, is -50.5 dBm. An example of the IF received spectrum is shown in Figure 5. Compared to the transmitted power of -10 dBm, the path loss for the 1 metre reference distance is -40.5dB. This loss can be assumed as free-space propagation loss and it matches with the result in [4] of 38 dB. The received signal is then sampled, stored and then plotted in Figure 6.

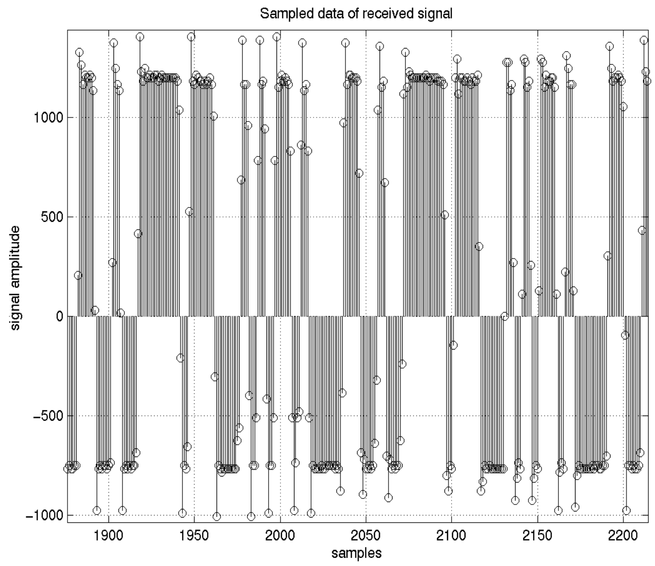

Figure 6: Received data sampled at 35 Msps

3.4 Synchronization of the measurement system

In general there are two main levels of synchronization in a coherent CDMA system; carrier and symbol (or bit) synchronization. The carrier synchronization in our system is achieved by using a common reference signal at both the TX and RX local oscillators (LO). This method eliminates the PLL required for carrier tracking, plus it reduces receiver hardware complexity.

For spread spectrum systems the transmitter and receiver waveforms are required to be synchronized. If two PN sequences are out of synchronization by one chip period, there will be insufficient signal energy for reliable data demodulation[15]. Initial synchronization or code tracking is achieved using a chip-match filter. Chip-match filtering of the sampled data sequence yields peaks at various sample points at the output, which is then used to determine the start of the PN sequence.

In a practical system the receiver does not know the chip timing for the desired user *a priori*. This chip-asynchronism leads to a fractional chip offset between the receiver's matched filter intervals and the chip timing for the user[6]. For example if signal is sampled at chip-rate, the worst case scenario corresponds to a half-chip offset, a SNR loss of 3 dB. In our measurement system the sampling rate is five times the chip-rate, and the SNR loss due to chip asynchronism is less severe. As stated in [6], the SNR loss due to fractional chip effects for a rectangular chip waveform is given by:

$$SNR = 10log[(\frac{1}{2m})^2 + (1 - \frac{1}{2m})^2]dB \tag{3}$$

where m/Tc is the sampling rate. For $m = 5$, the SNR loss is 0.86 dB and becomes less significant to signal-to-noise degradation. In addition, since data are processed offline, we can exploit the fact that the entire data sequence is available for timing recovery.

4 Physical Experiments

4.1 Non-linearity in antenna array system

One major concern in a smart antenna system is the non-linearity effects of the RF & IF chain on baseband digital beamforming [1]. In baseband digital beamforming, the received signal is usually assumed to be a linear superposition of signal vectors received by an antenna. For example, ignoring multipath

$$\mathbf{r(t)} = \sum_{i=1}^{N} s_i(t - \tau_i)\mathbf{a_i} + \mathbf{n(t)} \tag{4}$$

where N = total number of users
$\mathbf{a_i}$ = steering vector for user i
$s_i(t)$ = signal from user i
τ_i = time delay of user i
$\mathbf{n(t)}$ = additive white noise

Xue et al. demonstrated that non-linearities in the TX and RX chain distort the antenna beam pattern, and create larger side-lobes and a reduced null depth [1]. The result is limited interference cancellation and space diversity achievable by a smart antenna.

With our system, we would like to measure and quantify these non-linear effects with respect to a WCDMA system, and possibly devise a corrective method to minimize them. A setup with 2 mobiles and 1 antenna can be used to test the linear superposition of received signals. First each mobile is to transmit separately and the received data are served as individual references. The next set of data contains signals from both mobiles transmitting simultaneously. The linearity in latter received vector $r(t)$ can be verified by superpositioning each individual received signal.

We can also test non-linearity associated with the near far effect with the 2 mobiles and 1 transmitter setup by placing one mobile further away with the other, creating a strong interfering signal for the antenna to receive the weaker user.

4.2 Multipath measurements

Channel dispersion or multipath components provide multiple uncorrelated versions of the transmitted signal at the receiver, provided that their relative propagation delays exceed a chip period [9] [10]. The higher chip-rate in WCDMA means a reduced chip period, and more multipath components would be separated by more than one chip period, yielding more resolvable paths available for the receiver. To study WCDMA's receiver performance under the above conditions is one of the objectives of our measurement system.

In [9], an efficient suboptimal sequential detector is proposed. The proposed detector uses sequential hypothesis testing to dismiss the noise-only multipaths quickly, and reduces the amount of computations in spatial search of multipath signals with slight reduction of output SNR at 2-D Rake receiver.

Using the multi-element antenna array described in Figure 2, experiments can be performed to gather multipath data in WCDMA like environments. The actual performance of the spatial temporal receiver in [9] will be evaluated based on physical measurements.

Other relevant studies and experiments using our testbed are multi-user interference, radio propagation characteristics, as well as scattering and stability of spatial signature over time.

5 Preliminary Results and Conclusion

Two transmitters and one receiver were successfully established recently. Using one radio link a 7-MHz maximal length PN sequence with a length of 31 chips was transmitted over a small distance about 1 meter, without the use of a power amplifier at the TX. The IF-sampled data were stored on hard-disk, read, then plotted. Although there is need to refine offline signal processing procedures at this stage in our development, preliminary testing indicates that our low-cost modular design is functional at the hardware level. In the future we will be completing a second receiver link synchronized with the first. In the longer term we will determine the acquisition or synchronization requirements for separate transmit and receiver LOs.

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